REMARKS/ARGUMENTS

Claims 1-24 are currently pending in the present patent application. In an Office Action mailed on January 25, 2006, the Examiner allowed claims 11-24 and objected to claims 2, 3, 5, and 7-10, indicating these objected to claims were allowable if properly rewritten. Claim 1 was rejected as being anticipated by U.S. Patent No. 6,510,487 to Raza *et al.* ("Raza") and claims 4 and 6 were rejected as being obvious over Raza in view of U.S. Patent No. 6,777,979 to Zhu *et al.* ("Zhu").

The specification has been amended to correct several minor informalities and none of these amendments introduces any new matter into the application. Claims 2-10 have similarly been amended to correct several minor informalities in the form of typographical errors and also to replace the phrase "characterized in that" with the term "wherein." The term "wherein" has been utilized because it is more commonly accepted in U.S. practice and has been consistently construed by U.S. courts. None of these amendments to claims 2-10 narrows the scopes of any of these claims. Similarly, minor typographical errors have been corrected through amendments to claims 11, 15, 18, 20, and 24. None of these amendments narrows the scopes of any of the amended claims.

In the Office Action, the Examiner indicates claim 11 is allowed because none of the prior art of record teaches or suggests a memory device that operate in a serial mode during normal operation of the memory device and operates in a parallel mode during testing of the memory device. The Examiner appears to have believed independent device and system claims 15 and 20 included such limitations as well. Claims 15 and 20 have been amended to expressly recite such limitations and accordingly are now allowable.

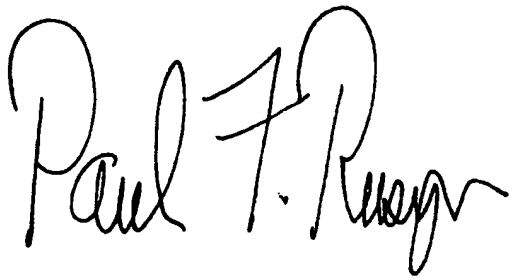
Claim 1 has been amended to recite, in part, a non volatile memory device architecture, for example of the Flash type, including an input/output interface operating according to a serial communication protocol. The interface includes a further pseudo-parallel communication portion which is used only during an electrical wafer sort test process prior to final testing of the assembled memory device architecture.

Neither Raza nor any of the other references or record, whether taken singly or in combination, teaches or suggests an interface that operates according to a serial communication protocol and includes a pseudo-parallel communication portion which is used only during an electrical wafer sort test process prior to final testing of the assembled memory device architecture. The Examiner recognized this fact in the Office Action. As a result, the combination of elements recited in amended claim 1 is allowable and dependent claims 2-10 are allowable for at least the same reasons as claim 1.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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